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MARTINE & PENILLA, LLP
710 LAKEWAY DRIVE
SUITE 170
SUNNYVALE, CA 94085

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/858,321	PACKER ET AL.	
	Examin r	Art Unit	
	Christopher E. Lee	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 May 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Substitute "316" by --216-- on page 4, line 1.

Substitute "328, 330, and 332" by --310, 312, and 314-- on page 9, line 18.

Substitute "304" by --306-- on page 10, line 10.

Substitute "334" by --314-- on page 11, line 5.

Substitute "602" by --402-- on page 12, line 21 and on page 13, line 7.

On page 15, line 6, fill in the patent application number.

Substitute "330" by --310-- on page 17, line 20.

Appropriate correction is required.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

Reference sign 216 in Fig. 2 is not used in the text disclosure.

Reference signs 512 and 508 in Fig. 5 are not used in the text disclosure.

Reference sign 600 in Fig. 6 is not used in the text disclosure.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because the direction of arrow "No" between Block 618 and Diamond 612 is reversed in light of the specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 28, 29 and 30 have been renumbered 27, 28 and 29, respectively.

5. Claim 9 is objected to because it recites the subject matter "the buses" in line 3 instead of "the bus". In fact, the subject matter "the buses" has not defined as said plural buses in line 2. Thus, it could be considered as "the bus" for the purpose of claim rejection based on a prior art. Appropriate correction is required.

6. Claim 10 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In the claim 10, it recites the claim 10 is a dependent claim of the claim 1. However, it could not be a dependent claim of the claim 1 because the claim 1 is a method claim. Therefore, the dependency is modified as a dependent claim of the claim 9 for the purpose of claim rejection based on a prior art.

7. Claim 21 is objected to because of the following informalities: In line 15, substitute --a **reset** and segment isolation controller-- for "a **rest** and isolation segment controller". Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over House et al. [US 5,274,783 A; hereinafter House] in view of Looi et al. [US 5,996,038 A; hereinafter Looi], Ehata [JP 2000181809 A] and IBM Technical Disclosure Bulletin ["Power Sequence Independent Expansion Bus Interface", TDB-ACC-NO: NN8606425, published by IBM, vol. 29, Issue No. 1, pages 425-426, on June 1, 1986; hereinafter IBM_TDB].

Referring to claim 1, House discloses a method for repeating communication signals by receiving said communication signals from one bus segment and outputting said communication signals to the other bus segment (See Abstract) in an I/O subsystem (i.e., computer system 10 in Fig. 1) having a plurality of bus segments (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1), each bus segment (e.g., segment of auxiliary SCSI bus in Fig. 1) having a set of devices (i.e., AUX-Bus peripheral devices 24 in Fig. 1) and a bus (i.e., Auxiliary Bus 28 of Fig. 1) that is coupled to said set of devices (See col. 4, lines 51-54), said I/O subsystem having at least one expander (e.g., Bus Extender 30 of Fig. 1), each expander being arranged to couple a pair of buses (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1) for propagating communication signals (See Fig. 1 and col. 4, line 63 through col. 5, line 2).

House does not expressly teach the steps of asserting a reset signal and resetting each expander and each device in response to said reset signal, i.e., a method steps for resetting bus segments to clear bus hang in said I/O subsystem.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein a method in said mechanism comprises a) asserting a reset signal (i.e., local bus reset signal) on a first bus segment (e.g., Expansion bus 61 in Fig. 1; See col. 4, lines 12-16); b) resetting each expander (i.e., bus expander bridge 60 of Fig. 1) coupled to said first bus segment (See col. 4, lines 4-6) and resetting each device (i.e., peripheral devices coupled to said bus 61 in Fig. 1) in said first bus segment (See col. 4, lines 16-20), i.e., a method steps for resetting bus segments (i.e., Buses 45, 64 and Expansion buses 51, 52, 61, 62 in Fig. 1) to clear bus hang in an I/O subsystem (i.e., computer system 10 of Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, in said method, as disclosed by House, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

House, as modified by Looi, does not teach each expander coupled to said first bus segment isolates said reset signal such that said reset signal is not propagated to the other bus segments.

Ehata discloses a SCSI control circuit (Fig. 2), wherein an expander (i.e., Reset-Condition Judging Circuit 7 of Fig. 2) coupled to a first bus segment (i.e., SCSI bus 3 of Fig. 2; e.g., as a hung-up SCSI device in Fig. 1) isolates a reset signal (i.e., RST signal of Fig. 2) such that said reset signal is not propagated to the other bus segments (e.g., not hung-up SCSI devices in Fig. 1; See col. 2 paragraph [0009] through col. 3, paragraph [0010]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said expander (i.e., Reset-Condition Judging Circuit), as disclosed by Ehata, in

said expander, as disclosed by House, as modified by Looi, so as to selectively reset only a bus segment (i.e., SCSI device) which has hung up by receiving said reset signal and resetting said hung-up bus segment when said hung-up bus segment is outputting a busy signal (See Ehata, col. 2, paragraphs [0005]-[0007]).

House, as modified by Looi and Ehata, does not expressly teach isolating all communication signals, and allowing propagation of communication signals between said first and other bus.

IBM_TDB discloses an expansion bus interface (See Figure), wherein c) for an expander (i.e., gate 3 in the Figure) coupled to a first bus segment (i.e., bus segment of local bus 13 in the Figure), c1) isolating all communication signals such that said expander (i.e., gate) prevents propagation of said communication signals between first bus (i.e., local bus 13 in the Figure) and other bus (i.e., external bus 18 in the Figure; See the second paragraph); c2) determining whether said other bus (i.e., external bus) is no longer hung (See the first paragraph, lines 9-10); c3) if said other bus is still hung, issuing a far-side reset signal (i.e., I/O RESET signal to I/O in the Figure) on said other bus to reset said other bus (See the first paragraph, lines 9-13); and c4) if said other bus is not hung, allowing propagation of communication signals between said first bus and said other bus (See the fourth paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said expander (i.e., gate 3 in the Figure), as disclosed by IBM_TDB, in expander, as disclosed by House, as modified by Looi and Ehata, so as to isolate said signals after isolating said reset signal for the advantage of prohibiting not hung-up bus segment (i.e., host system) inoperative from propagated faults in a hung-up bus segment (i.e., expansion unit) by said expander controller (i.e., circuit) which logically disconnects said hung-up bus segment (i.e., external bus in the external I/O unit) from said not hung-up bus segment (i.e., local bus in the host system) when a reset signal is asserted (i.e., when either a host system reset or an I/O unit power fault occurs; See IBM_TDB, the first paragraph).

Referring to claim 2, House, as modified by Looi, Ehata and IBM_TDB, discloses all the limitations of the claim 2 except that does not expressly teach if said other bus is still hung, operations b) and c) are repeated for other expanders coupled to each of said other buses.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have repeated said operations b) and c) for other expanders coupled to each of said other buses if said other bus is still hung, since it has been held that mere duplication of the essential working parts of said operations b) and c) for other expanders coupled to each of said other buses, involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

Referring to claim 3, Looi teaches each expander (e.g., bus expander bridge 60 of Fig. 1) enters into a reset isolation mode (i.e., reset state) in response to said reset signal (See col. 6, lines 26-31).

Referring to claim 4, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure) enters into a segment isolation mode (i.e., state of logically disconnected) to isolate all communication signals between said first bus and other bus (i.e., between local bus 13 and external bus 18 in the Figure; See the second paragraph).

Referring to claim 5, House teaches said I/O subsystem (i.e., computer system 10 in Fig. 1) is an SCSI I/O subsystem (See col. 4, lines 1-4) and wherein said other bus is no longer hung when said other bus is in a BUS FREE state (i.e., in fact that said computer system is using SCSI interface complying with SCSI standards implies that said other bus is no longer hung when said other bus is in a BUS FREE state).

Referring to claim 6, Looi teaches a host computer (i.e., processor 20 of Fig. 1) in said I/O subsystem (i.e., computer system 10 of Fig. 1) on said first bus segment (i.e., Expansion bus 61 in Fig. 1) asserts said reset signal on said first bus segment (See col. 4, lines 12-16 and 42-44).

Referring to claim 7, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure) exits said segment isolation mode (i.e., state of logically disconnected) when said other bus (i.e., external bus) is not

hung to allow said propagation of communication signals between said first bus and said other bus (See the fourth paragraph).

Referring to claim 8, Looi teaches said bus segments (i.e., Expansion bus 61 and Expansion bus 51 in Fig. 1) are reset one segment at a time from said first bus segment (i.e., Expansion bus 61 in Fig. 1; See col. 1, lines 6-10 and col. 6, lines 12-63).

11. Claims 9, 11, 12, 14, 15, 17, 19-21, 23, 24, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over House et al. [US 5,274,783 A; hereinafter House] in view of Ehata [JP 2000181809 A] and IBM Technical Disclosure Bulletin ["Power Sequence Independent Expansion Bus Interface", TDB-ACC-NO: NN8606425, published by IBM, vol. 29, Issue No. 1, pages 425-426, on June 1, 1986; hereinafter IBM_TDB].

Referring to claim 9, House discloses an expander device (i.e., Bus Extender 30 of Fig. 1) between a pair of bus segments (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1) in an I/O subsystem (i.e., computer system 10 in Fig. 1), each bus segment (e.g., segment of auxiliary SCSI bus in Fig. 1) having a set of devices (i.e., AUX-Bus peripheral devices 24 in Fig. 1) and a bus (i.e., Auxiliary Bus 28 of Fig. 1) that is coupled to said set of devices (See col. 4, lines 51-54), said expander device being arranged to couple said bus in said bus segments for communication in said I/O subsystem (See col. 4, lines 55-62), said expander device including: a first I/O interface circuit (i.e., transceiver 42 of Fig. 3) configured to be coupled to a first bus segment (i.e., bus segment of main bus 26 in Fig. 1), said first I/O interface circuit being adapted to interface input and output communication signals with said first bus segment (See col. 5, lines 34-42); a second I/O interface circuit (i.e., transceiver 44 of Fig. 3) configured to be coupled to a second bus segment (i.e., bus segment of auxiliary bus 28 in Fig. 1) and being adapted to interface said input and output communication signals with said second bus segment (See col. 5, lines 34-42); and an expander controller (i.e., transfer circuits 46, 48 and control logic 50 of Fig. 3) arranged to communicate said input and output communication signals between said first and second I/O interface

circuits, the expander controller being configured to control communication between said first and second bus segments (See col. 5, line 43 through col. 6, line 23).

House does not teach said expander controller includes a reset and segment isolation controller adapted to isolate a reset signal received on said first bus segment from propagating to said second bus segment, i.e., said expander device for isolating a reset between said pair of bus segments in said I/O subsystem.

Ehata discloses a SCSI control circuit (Fig. 2), wherein a reset and segment isolation controller (i.e., Inverter circuit 71 and OR circuit 72 in Fig. 2) adapted to isolate a reset signal (i.e., RST signal 6 of Fig. 2) received (See col. 2, paragraph [0004]) on a first bus segment (e.g., a hung-up SCSI device in Fig. 1) from propagating to a second bus segment (e.g., not hung-up SCSI device in Fig. 1), such that an expander device (i.e., SCSI control circuit in Fig. 2) for isolating a reset (i.e., RST signal) between said pair of bus segments in an I/O subsystem (i.e., SCSI bus system in Fig. 1; See col. 2 paragraph [0009] through col. 3, paragraph [0010]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reset and segment isolation controller (i.e., Inverter circuit and OR circuit), as disclosed by Ehata, in said expander controller, as disclosed by House, so as to selectively reset only a bus segment (i.e., SCSI device) which has hung up by receiving a reset signal and resetting said hung-up bus segment when said hung-up bus segment is outputting a busy signal (See Ehata, col. 2, paragraphs [0005]-[0007]).

House, as modified by Ehata, does not teach said expander controller isolates all signals to prevent propagation of said signals between said first and second bus segments after isolating a reset signal until said bus in said second bus segment is cleared from a hang condition.

IBM_TDB discloses an expansion bus interface (See Figure), wherein an expander controller (i.e., latch 2 and gate 3 in the Figure) isolates all signals to prevent propagation of said signals between a first bus segment (i.e., bus segment of local bus 13 in the Figure) and a second bus segment (i.e., bus segment of

external bus 18 in the Figure) when a reset signal is asserted (See the second paragraph) until the bus (i.e., external bus 18 in the Figure) in said second bus segment is cleared from a hang condition (See the third and fourth paragraphs; i.e., wherein in fact that the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus implies that said expander controller isolates all signals until the bus in said second bus segment is cleared from a hang condition).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said expander controller (i.e., latch 2 and gate 3 in the Figure), as disclosed by IBM_TDB, in said reset and segment isolation controller, as disclosed by House, as modified by Ehata, so as to isolate said signals after isolating said reset signal for the advantage of prohibiting a non-fault bus segment (i.e., host system) inoperative from propagated faults in a fault bus segment (i.e., expansion unit) by said expander controller (i.e., circuit) which logically disconnects said fault bus segment (i.e., external bus in the external I/O unit) from said non-fault bus segment (i.e., local bus in the host system) when a reset signal is asserted (i.e., when either a host system reset or an I/O unit power fault occurs; See IBM_TDB, the first paragraph) after isolating said reset signal so as to selectively reset only said fault bus segment (i.e., SCSI device) by receiving said reset signal and resetting said fault bus segment (See Ehata, col. 2, paragraphs [0005]-[0007]).

Referring to claim 21, House discloses an SCSI expander (i.e., Bus Extender 30 of Fig. 1) between a pair of bus segments (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1) in an SCSI I/O subsystem (i.e., computer system 10 in Fig. 1), each bus segment (e.g., segment of auxiliary SCSI bus in Fig. 1) having a set of devices (i.e., AUX-Bus peripheral devices 24 in Fig. 1) and a bus (i.e., Auxiliary Bus 28 of Fig. 1) that is coupled to said set of devices (See col. 4, lines 51-54), said SCSI expander being arranged to couple a first bus (e.g., main bus 26 in Fig. 1) in a first bus segment (i.e., bus segment of said main bus) and a second bus (i.e., auxiliary bus 28 in Fig. 1) in a second bus segment (i.e., bus segment of

said auxiliary bus), said SCSI expander being configured to repeat communication signals by receiving said communication signals from one SCSI bus segment and outputting said communication signals to the other SCSI bus segment (See Abstract), said SCSI expander comprising: a first SCSI I/O interface circuit (i.e., transceiver 42 of Fig. 3) adapted to interface communication signals with said first SCSI bus segment (i.e., bus segment of main bus 26 in Fig. 1; See col. 5, lines 34-42); a second SCSI I/O interface circuit (i.e., transceiver 44 of Fig. 3) adapted to interface said communication signals with said second SCSI bus segment (i.e., bus segment of auxiliary bus 28 in Fig. 1; See col. 5, lines 34-42); and an SCSI expander controller (i.e., transfer circuits 46, 48 and control logic 50 of Fig. 3) coupled to communicate said communication signals between said first and second SCSI I/O interface circuits, said SCSI expander controller being arranged to control communication between said first and second SCSI bus segments (See col. 5, line 43 through col. 6, line 23).

House does not teach said SCSI expander controller includes a reset and segment isolation controller adapted to isolate a reset signal received on said first bus segment from propagating to said second bus segment, i.e., said SCSI expander device for resetting said bus segments to clear bus hang in said SCSI I/O subsystem.

Ehata discloses a SCSI control circuit (Fig. 2), wherein a reset and segment isolation controller (i.e., Reset-Condition Judging Circuit 7 of Fig. 2) adapted to isolate a reset signal (i.e., RST signal 6 of Fig. 2) received (See col. 2, paragraph [0004]) on a first bus segment (e.g., a hung-up SCSI device in Fig. 1) from propagating to a second bus segment (e.g., not hung-up SCSI device in Fig. 1), such that an SCSI expander device (i.e., SCSI control circuit in Fig. 2) for resetting said bus segments to clear bus hang in said SCSI I/O subsystem (i.e., SCSI bus system in Fig. 1; See col. 2 paragraph [0009] through col. 3, paragraph [0010]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reset and segment isolation controller (i.e., Reset-Condition Judging Circuit),

as disclosed by Ehata, in said SCSI expander controller, as disclosed by House, so as to selectively reset only a bus segment (i.e., SCSI device) which has hung up by receiving a reset signal and resetting said hung-up bus segment when said hung-up bus segment is outputting a busy signal (See Ehata, col. 2, paragraphs [0005]-[0007]).

House, as modified by Ehata, does not teach said SCSI expander controller isolates all communication signals to prevent propagation of said communication signals between said first and second bus segments after isolating said reset signal until said second bus is in a BUS FREE state.

IBM_TDB discloses an expansion bus interface (See Figure), wherein an SCSI expander controller (i.e., latch 2 and gate 3 in the Figure) isolates all communication signals to prevent propagation of said communication signals between a first bus segment (i.e., bus segment of local bus 13 in the Figure) and a second bus segment (i.e., bus segment of external bus 18 in the Figure) when a reset signal is asserted (See the second paragraph) until said second bus is in a BUS FREE state (See the third and fourth paragraphs; i.e., wherein in fact that the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus implies that said expander controller isolates all communication signals until said second bus is in a BUS FREE state (viz., until the bus in said second bus segment is cleared from a hang condition)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said SCSI expander controller (i.e., latch 2 and gate 3 in the Figure), as disclosed by IBM_TDB, in said reset and segment isolation controller, as disclosed by House, as modified by Ehata, so as to isolate said signals after isolating said reset signal for the advantage of prohibiting a non-fault bus segment (i.e., host system) inoperative from propagated faults in a fault bus segment (i.e., expansion unit) by said expander controller (i.e., circuit) which logically disconnects said fault bus segment (i.e., external bus in the external I/O unit) from said non-fault bus segment (i.e., local bus in the host system) when a reset signal is asserted (i.e., when either a host system reset or an I/O unit power

fault occurs; See IBM_TDB, the first paragraph) after isolating said reset signal so as to selectively reset only said fault bus segment (i.e., SCSI device) by receiving said reset signal and resetting said fault bus segment (See Ehata, col. 2, paragraphs [0005]-[0007]).

Furthermore, the recitation that "an SCSI expander for resetting bus segments to clear bus hang in an SCSI I/O subsystem" which has been suggested by Ehata, has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *See Kropa v. Robie, 88 USPQ 478 (CCPA 1951).*

Referring to claims 11 and 23, IBM_TDB teaches if said second bus (i.e., External bus 18 in the Figure) is still hung, said expander controller (i.e., latch 2 and gate 3 in the Figure), which is said SCSI expander controller, issues a far-side reset signal (i.e., I/O RESET signal to I/O in the Figure) to said bus in said second bus segment to reset said second bus segment (See the fourth paragraph).

Referring to claims 12 and 24, IBM_TDB teaches said expander controller (i.e., latch 2 and gate 3 in the Figure) allows propagation of all signals between said first and second bus segments (i.e., local bus 13 and external bus 18 in the Figure) when said bus in said second bus segment (i.e., external bus) is cleared from said hang condition (See the fourth paragraph), which means said second bus is in said BUS FREE state.

Referring to claims 14 and 26, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure), which is said SCSI expander controller, enters into a segment isolation mode (i.e., state of logically disconnected) to isolate all signals between said first and second bus segments (i.e., between local bus 13 and external bus 18 in the Figure; See the second paragraph).

Referring to claim 15, House teaches said I/O subsystem (i.e., computer system 10 in Fig. 1) is an SCSI I/O subsystem (See col. 4, lines 1-4) and wherein said bus in said second segment is cleared from

said hang condition when said other bus is in a BUS FREE state (i.e., in fact that said computer system is using SCSI interface complying with SCSI standards implies that said other bus is cleared from said hang condition when said other bus is in a BUS FREE state).

Referring to claims 17 and 28, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure), which is said SCSI expander controller, exits said segment isolation mode (i.e., state of logically disconnected) when said second bus segment (i.e., external bus) is not hung, which means said second bus is in the BUS FREE state, to allow said propagation of communication signals between said buses in said first and second bus segments (See the fourth paragraph).

Referring to claim 19, House, as modified by Ehata and IBM_TDB, suggests said reset and segment isolation controller (i.e., Inverter circuit 71 and OR circuit 72 in Fig. 2; Ehata) generates a reset isolation signal (i.e., output from OR circuit 71 of Fig. 2; Ehata), which is provided to reset output buffers (i.e., AND circuit 73 of Fig. 2; Ehata) in said first and second I/O interface circuits (i.e., transceivers 42 and 44 in Fig. 3; House) to disable propagation of said reset signal (i.e., RST signal 6 of Fig. 2; Ehata) to said first and second bus segments (i.e., bus segments of main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1; House).

Referring to claim 20, House, as modified by Ehata and IBM_TDB, suggests said reset and segment isolation controller (i.e., LATCH 2 in the Figure; IBM_TDB) generates a segment isolation signal (i.e., I/O reset signal from latch 2 in the Figure; IBM_TDFB), which is provided to all output buffers in said first and second I/O interface circuits (i.e., GATE 3 of the Figure; IBM_TDB) to disable output of said communication signals (See IBM_TDB, the third and fourth paragraphs) from said first and second I/O interface circuits (i.e., transceivers 42 and 44 in Fig. 3; House) to said first and second bus segments (i.e., bus segments of main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1; House).

12. Claims 10, 13, 16, 18, 22, 25, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over House [US 5,274,783 A] in view of Ehata [JP 2000181809 A] and IBM_TDB ["Power

Sequence Independent Expansion Bus Interface", TDB-ACC-NO: NN8606425, published by IBM, vol. 29, Issue No. 1, pages 425-426, on June 1, 1986] as applied to claims 9, 11, 12, 14, 15, 17, 19-21, 23, 24, 26 and 28 above, and further in view of Looi [US 5,996,038 A].

Referring to claims 10 and 22, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 10 and 22, respectively, except that does not teach said expander controller, which is said SCSI expander controller, is adapted to reset said expander device in response to said reset signal and wherein all devices in said first bus segment reset in response to said reset signal such that said bus in said first bus segment is cleared from said hang condition, which means said first bus is in said BUS FREE state.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein an expander controller (e.g., bus expander bridge 50 of Fig. 1) is adapted to reset an expander device (e.g., bus expander bridge 0 60 of Fig. 1) in response to a reset signal (See col. 6, lines 26-31) and wherein all devices (e.g., peripheral devices coupled to said bus 61 in Fig. 1) in a first bus segment (i.e., Expansion bus 61 in Fig. 1) reset in response to said reset signal such that a bus in said first bus segment is cleared from a hang condition (See col. 6, lines 31-35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Thus, House, as modified by Ehata, IBM_TDB and Looi, teaches said first bus is in said BUS FREE state (i.e., in fact that House teaches said computer system is using SCSI interface complying with SCSI standards, and said bus in said first bus segment is cleared from said hang condition implies that said first bus is in a BUS FREE state).

Referring to claims 13 and 25, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 13 and 25, respectively, except that does not teach said expander controller, which is said SCSI expander controller, enters into a reset isolation mode in response to said reset signal. Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein an expander controller (e.g., bus expander bridge 50 of Fig. 1) enters into a reset isolation mode (i.e., reset state) in response to said reset signal (See col. 6, lines 26-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Referring to claims 16 and 28, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 16 and 28, respectively, except that does not teach a host computer on said first bus segment in said I/O subsystem, which is said SCSI I/O subsystem, asserts said reset signal on said first bus segment.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein a host computer (i.e., processor 20 of Fig. 1) in an I/O subsystem (i.e., computer system 10 of Fig. 1) on a first bus segment (i.e., Expansion bus 61 in Fig. 1) asserts a reset signal on said first bus segment (See col. 4, lines 12-16 and 42-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Referring to claims 18 and 29, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 18 and 29, respectively, except that does not expressly teach said bus segments are reset one segment at a time from said first bus segment.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein bus segments (i.e., Expansion bus 61 and Expansion bus 51 in Fig. 1) are reset one segment at a time from a first bus segment (i.e., Expansion bus 61 in Fig. 1; See col. 1, lines 6-10 and col. 6, lines 12-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Conclusion

13. The Examiner refers to Ehata [JP 2000181809 A] reference as a prior art for the claim rejection(s) in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicant(s). However, the Examiner cautions the Applicant(s) that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Bus Fault Isolation on Serial Bus,

Luebke et al. [US 5,999,389 A] disclose repeater for bus with bus fault isolation.

With regard to Bus Reset Method,

Bruckert et al. [JP 403184109 A] disclose target designation method for data processor.

Wada [US 6,519,713 B1] discloses magnetic disk drive and SCSI system employing the same.

Benson et al. [US 6,567,879 B1] disclose management of resets for interdependent dual small computer standard interface (SCSI) bus controller.

With regard to Bus Repeater,

Aoki et al. [JP 407281994 A] disclose bus repeater.

Murai [JP 409022395 A] discloses SCSI bus repeater.

Nomura [US 6,448,810 B1] discloses bi-directional bus-repeater controller.

Tuccio [US 5,819,104 A] discloses disk array memory system having bus repeater at disk backplane.

Scholhamer et al. [US 6,636,921 B1] disclose SCSI repeater circuit with SCSI address translation and enable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100